CLAIMS

1. A method of jitter compensation of a phase locked loop frequency synthesizer by means of a variable delay, the method characterized in that the jitter is compensated prior to a signal being subject to jitter is passed through a non-linearity, the jitter compensating variable delay being realized by means of a tapped delay line.

2. The method according to claim 1 characterized in that each of a plurality of integer divisors are selected according to a fractional pattern, representing fractional weighting of the integer divisors, generated by a ΣΔ modulator from a fractional setting input.

3. The method according to claim 1 or 2 characterized in that a fraction of a first and a second integer is determined by a binary fractional pattern, for selecting the first or the second integer, generated by a ΣΔ modulator from a fractional setting input.

4. The method according to claim 2 or 3 characterized in that the tapped delay line is controlled by means of control signals derived from the ΣΔ modulator.

5. The method according to claim 4 characterized in that a control signal for controlling the tapped delay line is determined by integrating and scaling an error signal being the difference between a signal representing the fraction and a signal carrying the fractional pattern.

6. The method according to any of claims 1-5 characterized in that the tapped delay line com-

prises a plurality of capacitors with capacitances proportional to successive powers of 2.

7. The method according to claim 5 or 6 characterized in that the control signal carries a binary number whose bit representation connects or disconnects capacitors of the tapped delay line with respective capacitances corresponding to bit positions of the binary representation.

8. The method according to any of claims 1-5 characterized in that the tapped delay line comprises a plurality of serially connected delay elements.

9. The method according to claim 5 or 8 characterized in that the control signal carries a representation for connecting or disconnecting a delay element of the tapped delay line to either the input or output of the tapped delay line.

10. The method according to claim 9 characterized in that the control signal carries a bit representation for connecting or disconnecting a delay element output to the output of the tapped delay line.

11. The method according to claim 9 characterized in that the control signal carries a bit representation for connecting or disconnecting a delay element input to the input of the tapped delay line.

12. The method according to any of claims 1-11 characterized in that the non-linearity is included in or is a phase or frequency detector.

13. The method according to any of claims 1-12 characterized in that the output signal of the

tapped delay line is input to the phase or frequency detector.

14. The method according to any of claims 1-13 characterized in that at least one of

- a reference frequency signal,
- a frequency divided output signal of a voltage controlled oscillator,
- a frequency divided output signal of the frequency synthesizer,

is input to and delayed by the tapped delay line.

15. The method according to any of claims 1-12 characterized in that the output signal of the tapped delay line is input to frequency dividing circuitry.

16. The method according to any of claims 1-12 and 15 characterized in that at least one of

- an output signal of a voltage controlled oscillator, and
- an output signal of the frequency synthesizer

is input to and delayed by the tapped delay line.

17. A phase locked loop frequency synthesizer with jitter compensation by means of a variable delay, the frequency synthesizer characterized by a tapped delay line compensating the jitter prior to a signal being subject to jitter is passed through a non-linearity.

18. The frequency synthesizer according to claim 17 characterized by a $\Sigma\Delta$ modulator for generating or a storing element for pre-generated storing of a fractional pattern representing fractional weighting of a

plurality of integer divisors, the fractional pattern selecting one integer divisor, out of the plurality of integer divisors, at a time to be active.

19. The frequency synthesizer according to claim 17 or 18 characterized by a ΣΔ modulator for generating or a storing element for pre-generated storing of a binary fractional pattern for determining a fraction of a first and a second integer, the binary fractional pattern selecting the first or the second integer, the binary fractional pattern being generated from or restored from a fractional setting input.

20. The frequency synthesizer according to claim 19 characterized by control means for controlling the tapped delay line by means of one or more control signals derived from the ΣΔ modulator.

21. The frequency synthesizer according to claim 20 characterized by an integrator integrating and scaling an error signal being the difference between a signal representing the fraction and a signal carrying the binary fractional pattern, the integrator output signal being a signal for controlling the tapped delay line.

22. The frequency synthesizer according to any of claims 17-21 characterized in that the tapped delay line comprises a plurality of capacitors with capacitances proportional to successive powers of 2.

23. The frequency synthesizer according to claim 21 or 22 characterized by switches for connecting or disconnecting capacitors of the tapped delay line, wherein respective capacitances corresponding to bit positions of a binary representation of a binary number are connected or

disconnected, the binary number being carried by the one or more control signals.

24. The frequency synthesizer according to any of claims 17-21 characterized by the tapped delay line comprising a plurality of serially connected delay elements.

25. The frequency synthesizer according to claim 21 or 24 characterized by one or more switches for connecting or disconnecting one or more delay elements to the input or output of the tapped delay line according to a bit representation, the bit representation being carried by a control signal.

26. The frequency synthesizer according to claim 25 characterized by the one or more switches each connecting or disconnecting a delay element output to the output of the tapped delay line.

27. The frequency synthesizer according to claim 25 characterized by the one or more switches each connecting or disconnecting a delay element input to the input of the tapped delay line.

28. The frequency synthesizer according to any of claims 17-27 characterized in that the non-linearity is included in or is a phase or frequency detector.

29. The frequency synthesizer according to any of claims 17-28 characterized in that the output signal of the tapped delay line is input to the phase or frequency detector.

30. The frequency synthesizer according to any of claims 17-29 characterized in that at least one of

- a reference frequency signal,

- a frequency divided output signal of a voltage controlled oscillator,
- a frequency divided output signal of the frequency synthesizer,

is input to and delayed by the tapped delay line.

31. The frequency synthesizer according to any of claims 17-28 characterized in that the output signal of the tapped delay line is input to frequency dividing circuitry.

32. The frequency synthesizer according to any of claims 17-28 and 31 characterized in that at least one of

- an output signal of a voltage controlled oscillator, and
- an output signal of the frequency synthesizer

is input to and delayed by the tapped delay line.

33. A radio communications system characterized by means for carrying out the method in any of claims 1-16.

34. A radio communications system characterized by one or more frequency synthesizers according to any of claims 17-32.